High Rate Digital Demodulator ASIC

Andrew Gray Parminder Ghuman Salman Sheikh
JPL/Caltech NASA/GSFC NASA/GSFC
Steve Koubek Scott Hoy
Lockheed-Martin Lockheed-Martin

ABSTRACT

The architecture of the High Rate (600 Mega-bits per second) Digital Demodulator (HRDD) ASIC capable of demodulating BPSK and QPSK modulated data is presented in this paper. The advantages of all-digital processing include increased flexibility and reliability with reduced reproduction costs. Conventional serial digital processing would require high processing rates necessitating a hardware implementation other than CMOS technology such as Gallium Arsenide (GaAs) which has high cost and power requirements. It is more desirable to use CMOS technology with its lower power requirements and higher gate density. However, digital demodulation of high data rates in CMOS requires parallel algorithms to process the sampled data at a rate lower than the data rate.

INTRODUCTION

The data rates for NASA missions are increasing very rapidly. In order to process these high data rates high performance processing hardware is required. For baseband data processing, there exists inexpensive PCI-based solutions but for RF processing, the current solutions are based on either all analog or mixed technology with flexibility offered only at great cost and size. For an all-digital solution, the sampling rate of passband data is at least 4 times the data rate [1]. That is a minimum of 4 samples per symbol are required in order to demodulate the modulated data and then perform carrier recovery, symbol detection, and symbol timing recovery with an all-digital receiver. For 300 Megabit data this is 1,200 million samples per second. Using conventional serial processing techniques the clock cycle of the digital receiver would have to be 1,200 MHz. This is too high to implement in any current technology and with even higher data rates planned for the future, an alternative method to demodulate BPSK/QPSK data needed to be found that would utilize parallel processing. The multirate signal processing algorithms [2,3] developed by NASA's Goddard Space Flight Center (GSFC) and the Jet Propulsion Laboratory (JPL) that accomplish this require the demodulator ASIC to run at a clock rate that is only one-fourth the data rate. For example, for a 300 Megabit data rate, the clock rate required for the HRDD ASIC is 75 MHz, which can easily be obtained with CMOS technology. This all-digital implementation allows more flexibility than is currently possible with analog or mixed signal processing. Finally, as will be demonstrated in this paper, this high rate digital demodulator can be used with an off-the-shelf A/D and a flexible analog front end, both of which are numerically computer controlled, to

produce a very flexible, low cost high rate digital receiver.

HRDD ARCHITECTURE

The design approach for the high rate digital demodulator consisted of algorithmic development, software simulations, development of a hardware prototype in reprogrammable hardware, and finally development of a single 800K gate CMOS ASIC. A summary of the design process used is illustrated in Figure 1.

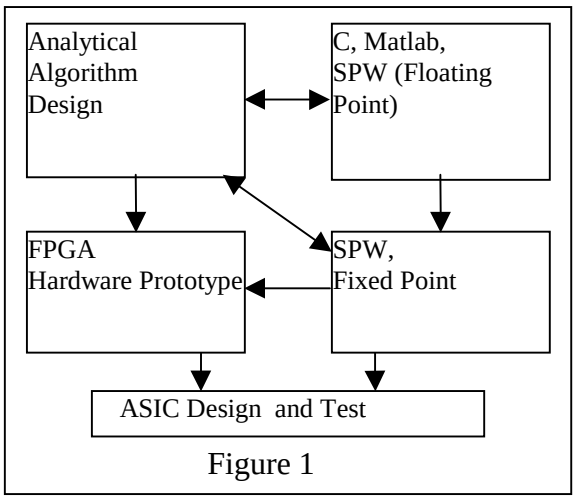

Figure 1

Figure 2 depicts a block diagram of the digital demodulator ASIC. Two identical ASICs will be required in the digital receiver, one to perform in-phase (I) channel processing and one to perform quadrature (Q) channel processing. The input signals to the digital demodulator ASICs are 8 parallel 8 bit A/D samples that are demuxed to obtain 16 parallel 8-bit samples. Optionally, these samples can be Gray decoded as well as converted from unsigned numbers to signed numbers.

These 16 samples are digitally mixed with a 10 bit mixer bank in both the I and Q channels and converted to the frequency domain via a modified 32-point DFT (GDFT). The DFT is modified to eliminate calculating the frequency components of the double frequency term resulting from mixing the BPSK/QPSK modulated data to baseband [4,5]. The resulting outputs of the GDFT are 15 parallel 13 bit samples. These samples then pass through the lowpass/detection filter which filters out the double frequency term while performing symbol detection filtering followed by the symbol time recovery phase corrector. The coefficients for the lowpass/ detection filter are programmable to

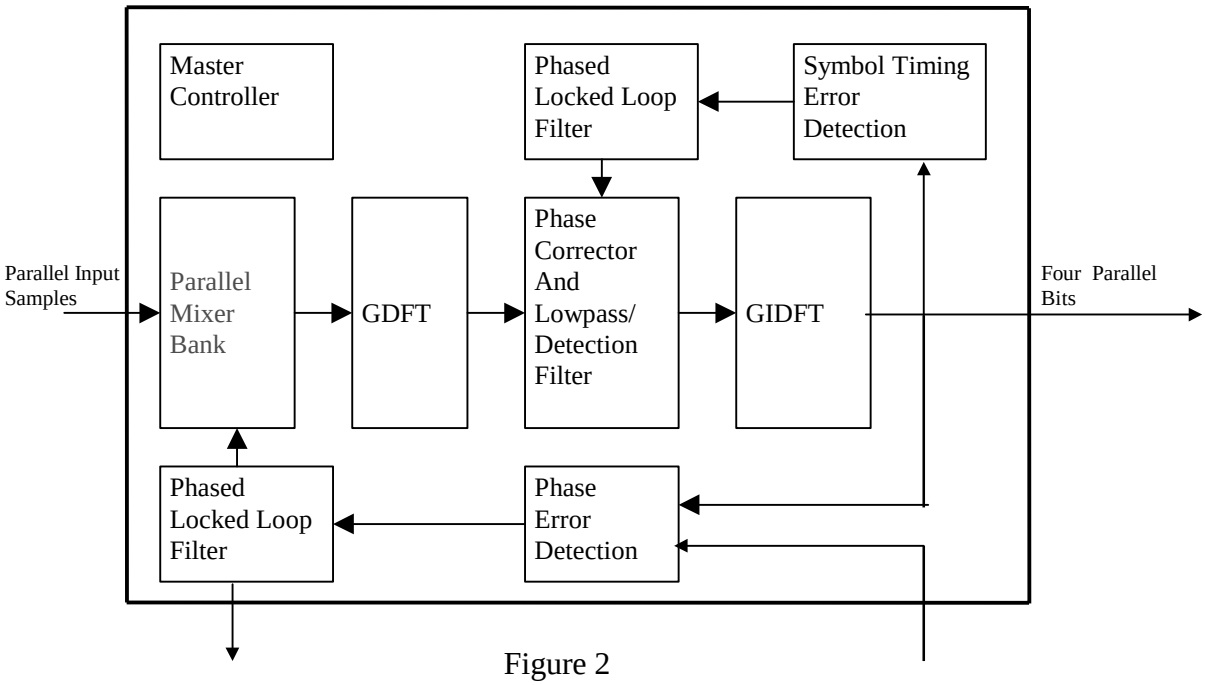

Figure 2

accommodate different transmitted pulse shapes and channel distortions of the pulse shape. The data then goes input to a modified 32 point IDFT (GIDF) that converts the data back to the time domain.

During all of these operations there are always sixteen valid samples being processed in parallel. That is, four information bits are being processed simultaneously and four information bits are output by the GIDFT on both the I and Q channel every clock cycle during QPSK demodulation. During BPSK demodulation, information bits are present at the output of the GIDFT on the I channel with no information bits present on the output of the Q channel.

The output of the GIDFT is then fed to two digital phase locked loops: the symbol time recovery DPLL and the Costas DPLL. The symbol time recovery DPLL is composed of a symbol timing error detector and a loop filter that has an output resolution of 8 bits that feeds back into the symbol time recovery phase corrector. The Costas DPLL is composed of a BPSK/QPSK phase error detection algorithm followed by a loop filter that feeds back into the ten bit mixer bank. Two different preprogrammed loop filter bandwidths are chosen for each DPLL by the internal master controller depending upon the state of the Costas DPLL, which is either in a locked state or acquisition state. Up to eight different preprogrammed loop filter bandwidths can be chosen in real-time externally for both DPLLs. Due to testing of fixed-point software models as well as the hardware prototype, it was determined that the delay caused by pipelining the hardware in order for it to run as fast as possible had the potential to create unacceptable degradation in the performance of the two DPLLs. The degradation is greatest when processing low data rates. To minimize the delay from hardware pipelining it was determined that the ASIC would always be clocked at the maximum rate possible regardless of the data rate. To achieve this two internal clocks which drive internal logic and arithmetic operations are necessary. These are the ASIC or system clock, and the data valid clock operating at one-fourth the data rate. For example, if the system clock is running at ten times the data valid clock, the effective delay is one-tenth the delay that would result if the system clock were operating at one-fourth the data rate. This method minimizes the digital signal propagation delay through the synchronous portion of the design as well as through the feedback paths of both DPLLs. It should be noted that there is no requirement that the system clock be an integer multiple of the data clock. Therefore it is possible to have a non-integer sample delay (on average) in the logic. This design requires additional hardware and testing is more complex, but the method is an effective way of minimizing the effective pipline delay in the ASIC when the data rates dictates a data clock slower than the system clock.

To perform Costas DPLL acquisition and lock detection as well as other monitoring functions the output of the GIDFT from both channels is input to the master controller. The master controller's main functions are to determine if the Costas loop is in lock and to remove effective Doppler between the incoming signal and the digital mixer frequency by sweeping the digital mixer frequency until it approximately matches that of the incoming sampled frequency (aided acquisition). The user also has flexibility in programming most of the parameters in the lock detection and acquisition algorithms. These parameters include the filter order for the filter used to remove noise on the lock detection signal, the threshold the lock

detection signal is compared with to determine lock, sweep frequency, and sweep rate. In addition other parameters of the lock detection algorithm which are designed to minimize probability of false lock may be programmed. The master controller also outputs the status of the lock detection and acquisition algorithms. The ASIC incorporates enough flexibility in I/O and control that the entire phase/frequency acquisition algorithm, along with both DPLL operations, can be accomplished externally by other computational devices if different methods of carrier phase recovery and symbol timing recovery are desired. There is also a power compensator algorithm in the master controller used for demodulating differential power QPSK and differential data rate QPSK data. This algorithm is used if the power on the I and Q channels is different when transmitted but needs to be equal after demodulation .

RECEIVER ARCHITECTURE

Figure 3 illustrates the block diagram of the receiver architecture. Two identical HRDD ASICs are used in the digital BPSK/QPSK receiver. Both ASICs, the A/D converter, and supporting digital hardware are designed on a single PCI card.

The analog front end is used to mix the data to an appropriate intermediate frequency as well as filter that data prior to the A/D converter. The analog front end is also designed to operate on a single PCI card. The data is sampled at a rate four times the data rate and demultiplexed using two identical 4-bit GaAs 1-8 multiplexer/demultiplexers developed by GSFC. The data is then sent to the two HRDD ASICs, which demultiplex the data by 2, perform demodulation, bit synchronization, and send 4 parallel symbols to the next subsystem. The high rate digital receiver integrated on two PCI cards has the following features:

- Demodulates BPSK, QPSK, Differential power QPSK, OQPSK, and differential data rate QPSK
- Can demodulate data in the range of 10 to 300 + Mega-symbols per second
- Numerically controlled DPLL filter bandwidths
- Can compensate for Doppler in the

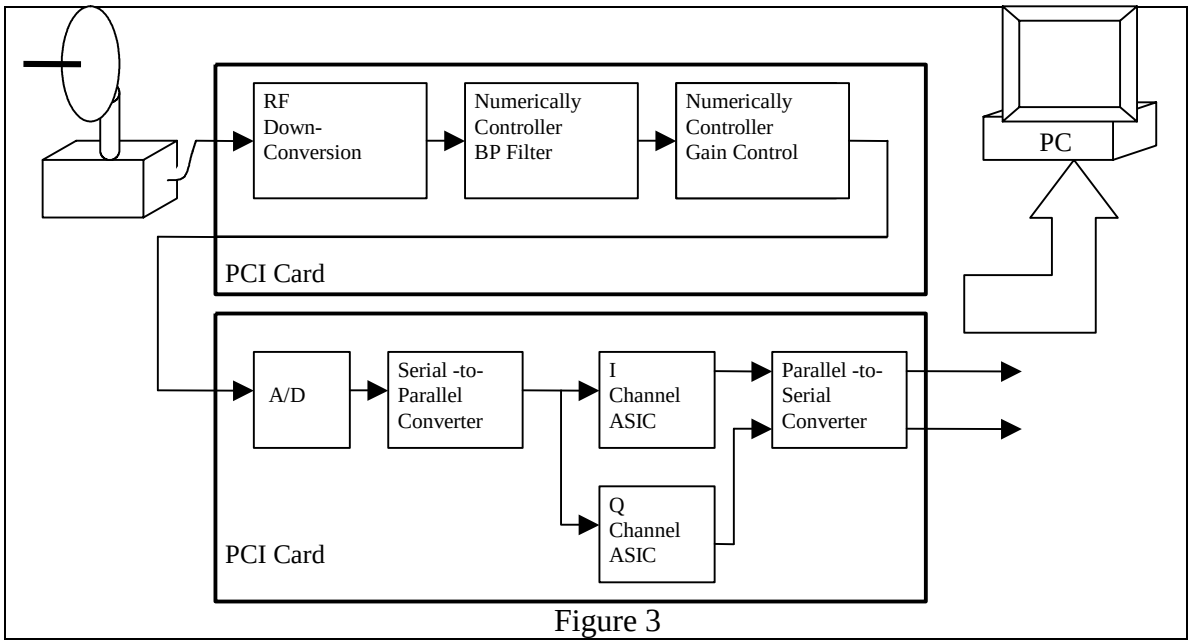

Figure 3

range of +/- 160kHz in the X band internally with the option to be done externally

- The HRDD can demodulate data with SNRs lower than 2dB (Eb/No)
- Can process Gray encoded data and normal signed and unsigned data
- The implementation loss for the receiver using HRDD ASIC is approximately 1dB
- Provides programmable lowpass /detection filter coefficients
- Provides constant gain soft symbol output from both channels for input to Viterbi decoders

CONCLUSION

This paper has provided an overview of the hardware architectures used to develop a high rate CMOS demodulator ASIC. It has also demonstrated how this ASIC will be used in a digital receiver that provides great improvement in size, cost, and flexibility over currently available high rate BPSK/QPSK receivers. The ASIC is scheduled to begin testing in the Lab at GSFC in the Fall of 1998. The operational prototype of the receiver presented in this paper is scheduled to begin testing in January 1999. The I/O and controlling functions of the demodulator ASIC have been made as flexible as possible given package size and pin count constraints. In addition to the flexibility outlined in this paper the demodulator ASICs can be used with additional digital hardware to demodulate 8-PSK and potentially other modulation schemes as well. For further information please contact Parminder Ghuman at NASA/GSFC.
(ghuman@vlsi.gsfc.nasa.gov)

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